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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,410	02/04/2002	Christopher W. Hill	3380.1US (97-842.1)	8302

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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/067,410	HILL ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 8-10, 12-14, 18-20, 23 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (US 6,020,259, submitted by applicant) in view of Danek et al (US 6,699,530).

In re claims 1, 8, 14, 20, 27 and 28, Chen et al. in Figs. 4-7 and related text, teach the claimed method, comprising:

- causing a chemical reaction (i.e. *TiCl4 reacts with S*, col. 3, lines 2-19) adjacent to a surface of one exposed, doped area 30 (i.e. source and drain regions) of a semiconductor device structure to *selectively deposit* (col. 3, line 3) titanium silicide or contact material 36 (i.e. $TiSi_2$) by using a *CVD process* (col. 3, line 4) thereon without reacting material of the one exposed, doped area *because* the formation of the $TiSi_2$ does *not consume* the underlying doped silicon region 30; and
- after causing the chemical reaction, subsequently blanket depositing an interconnect material 38 (i.e. a barrier, *TiN*) by using a *CVD process* (col. 3, lines 20 –22) onto the metal silicide or the contact material 36 *after* with causing the chemical reaction (col. 3, lines 20-23).

Chen et al. is silent as to the interconnect material (TiN) being deposited *insitu* with causing the chemical reaction. Chen et al., however, do imply a desirability of depositing the interconnect material insitu (i.e. in the same chamber) with causing the chemical reaction because Chen et al. teach that the interconnect material 38 is *subsequently* formed after the chemical reaction, wherein the term "subsequently" imply without removing the semiconductor device structure to a different chamber to carry out depositing the interconnect material. In addition, the deposition of both the titanium silicide 36 and the interconnect material 38 are performed using a same technique, i.e. the CVD process (col. 3, lines 2-4 and 20-22).

In fact, insitu deposition has been widely used in the art for the purpose of eliminating contamination, as evidenced by Danek et al. Danek et al., teach *insitu* depositing an interconnect material 102 onto a barrier material 100 for the advantages of reducing the amount of contamination and saving manufacturing time (Fig. 1 and col. 3, lines 23-40).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to *subsequently insitu* deposing the interconnect material, as taught by Danek et al, onto the metal silicide *after* the chemical reaction in Chen et al., since by this manner it would reduce the amount of contamination and saving manufacturing time (col. 3, lines 23-40, Danek et al.).

In re claims 9, 10, 25 and 26, Chen et al. teach that depositing the interconnect material (TiN) comprises *blanket* depositing the interconnect material (col. 3, lines 20-23) and *patterning* the interconnect material by removing the excess interconnect material from outside of the contact hole (Figs.6-7).

In re claims 12, 13 and 23, Chen et al. further teach depositing an electrically conductive layer 40 over the interconnect material 38 and patterning the electrically conductive layer 40 by removing the excess electrically conductive layer from the outside of the contact hole (Fig.7).

In e claims 18-19, Chen et al. further teach that depositing the interconnect material comprises reacting a metallic precursor (i.e.$TiCl_4$ or titanium tetrahalide) with a reactant comprising an activated species (i.e. N_2) (col. 3, lines 20-24).

3. Claims 2-5 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Danek et al as applied to claims 1, 8-10, 12-14, 18-20, 23 and 25-28 above, and further in view of Chang et al. (US 5,043,299).

In re claims 2-4 and 21, Chen et al in view of Danek et al teach the claimed method, as stated above, but fails to teach exposing said at least one exposed, doped area of the semiconductor device structure to a plasma comprising an activated species of at least one of nitrogen, hydrogen, and ammonia; and cleaning the semiconductor device structure.

Chang et al., in an analogous art of selective deposition, teach a pre-deposition preparation by exposing the exposed, doped area of the semiconductor device structure to plasma comprising an activated species of at least one of nitrogen and hydrogen (Fig.1 and text in col. 3, lines 14-26; col. 4, lines 10-15); and cleaning the semiconductor device structure (col.7, lines 1-11) for the purpose of removing contaminants including undesirable oxide and moisture (col.2, lines 15-28; col.6, lines 48-61).

Therefore, one of the ordinary skill in the art, at the time of the invention was made, would have been motivated to expose the exposed, doped area of semiconductor device structure of Chen et al in view of Danek et al. by the plasma comprising either nitrogen or hydrogen and

cleaning the semiconductor device structure, as taught by Chang et al., since by doing so it would be beneficial to the subsequent selective deposition. (col.2, lines 15-28; col.6, lines 48-61, Chang et al)

In re claim 5, Chen et al in view of Danek et al. and Chang et al. further teach that said cleaning includes employing a cleaning agent comprising chlorine. Particularly, Chang et al. indicate using a halogen-containing gas, which at least would include chlorine and fluorine, for the cleaning purpose. (col.7, lines 5-6).

In re claim 22, Chen et al in view of Danek et al. and Chang et al. do not teach exposing the semiconductor device structure to a nitrogen-ammonia plasma. However, the selection of the cleaning plasma for said exposing step is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious). For example, the cleaning plasma can be selected for the particular surface to be cleaned, dependent upon the material of the particular surface. (col.3, lines 14-26, Chang et al.) In this case, the applicant is required to demonstrate the criticality, generally by showing that the claimed plasma would achieve unexpected results relative to the prior art. See M.P.E.P. 2144.05 III.

4. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Danek et al. as applied to claim 1 above, and further in view of Kolar et al. (US 5,162,259).

Chen et al. in view of Danek et al. teach the claimed method, as stated above, but fails to teach cleaning the semiconductor device structure after said depositing said metal silicide, wherein said cleaning includes employing a cleaning agent comprising at least one of chlorine, hydrochloric acid, and hydrofluoric acid.

Kolar et al. in an analogous art teach forming a silicide layer 40 followed by cleaning the semiconductor device structure employing a cleaning agent comprising hydrochloric acid, prior to depositing an interconnect material 38. (Fig.4 and text in col. 21-23)

Therefore, one of the ordinary skill in the art, at the time of the invention was made, would have been motivated to utilize said hydrochloric acid as cleaning agent as taught by Kolar et al., in the method of Chen et al. in view of Danek et al. to clean the surface of said deposited metal silicide and then to deposit said interconnect material, since by doing so it would improve the adhesion between adjacent layers.

5. Claims 11 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Danek et al. as applied to claim 1 above, and further in view of Kim et al. (US 5,821,164).

Chen et al. in view of Danek et al. do not teach *selectively* depositing the interconnect material (TiN).

However, using selective deposition for forming TiN in a contact hole has been widely used in the art, as evidenced by Kim et al. (col. 4, lines 24-27).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use the selective deposition, as taught by Kim et al., for forming the interconnect material of Chen et al in view of Danek et al., since by this manner it would

provide a better means for controlling the desired location and thickness of the interconnect material.

6. Claims 15-17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Danek et al. as applied to claim 1 above, and further in view of Shinriki et al. (US 6,001,729).

Chen et al. teach that causing the chemical reaction comprises reacting a metallic precursor (i.e. *$TiCl_4$ or titanium tetrahalide*) with silicon (col. 3, lines 2-19) but is silent as to the silicon source being a silicon compound.

Shinriki et al., however, teach causing a chemical reaction via using metallic precursor (i.e. $TiCl_4$) with a silicon compound (i.e. SiH_4 or silane) (col. 12, lines 37-39) adjacent to a surface of one exposed, doped area 38 of a semiconductor device structure to selectively deposit titanium silicide.

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to use the silicon compound, as taught by Shinriki et al., as the silicon source of Chen et al., since by this manner it would satisfactory cause the chemical reaction to form the titanium silicide.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (7:30 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
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HSIEN-MING LEE
PRIMARY EXAMINER

Oct. 12, 005